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(H. F. H. J. C. K. E.)

(拾次項1) キ田は基子の磁子軌の直に 二道は基子の磁子と電気的に結合するたの外部磁子軌と、キ道は基子の磁子軌の直へ還元して外部へと向く内部磁子軌への修成のための外部磁子軌と、内部磁子軌と外部磁子軌とを導通する接点リード板とを一体としたリード板を形成面、他は修成板面を介して、結合してはけており、且つ、回路基板等への実装のためのキ田からなる外部磁板を同定修成のをリードの外側磁子軌に導通させ、少なくとも同定キ田からなる外部磁板の一部に外部磁子軌より外部に突出させて設けていることを特徴とする回路基止型キ道体装置。

(図 2) 図 1 において、半導体素子の素子は半導体素子の素子面の一対の辺の両中心配向に於て配座されており、リード線は接点の素子を挟むように対向し配座一対の辺に接し合けられていることを特徴とする接点防止型半導体素子。

(図3項3) と導体素子の端子と電気的に接続するた
めの内部端子部と、力配区画と接続するための力配端子
部と、上記内部端子部と力配端子部とを導通する接続リ
ード部とを一体とし、該力配端子部を、接続リード部を
介して、リードフレーム面から突出する一方側面に突出
させ、対向し先端部同士で導通部を介しては接続する一対
の内部端子部を形成しており、且つ、各力配端子部の
先端で、接続リード部と導通し、一体として全体を露出
「る外ね部を設けていることを特徴とするリードフレ

【図2項4】 本図は素子の端子部の断面に、本図は素子1端子と電気的に接続するための内部端子部と、半導体子の端子部の面へ重交して外部へと向く外部端子部との成のための外部端子部と、既記内部端子部と外部端子部とを接続するはかりード部とを一体とした複数のリード部とを、給線用導線部を介して、接続して設けてお、且つ、既記基板等への実装のための半田からなる外電極を既記複数の各リードの外側端子部に導絡させ、なくとも既記半田からなる外側電極の一部は既記部より外部に突出させて設けている製造禁止型半導体装置の1例であつて、少なくとも、(A)エッチング加工で、半導体素子の端子と電気的に接続するための内部端子部と、外部部部とを形成するための外部端子部と、両者部端子部と外部端子部とを接続するはかりード部とを一体とし、該外部端子部を、該かりード部を介して、ードフレーム面から重交する一方所部に突出させ、外側電極同士と導絡部を介して接続する一方の内側部とを接続設けており、且つ、各外側端子部の外側で、ード部と導絡し、一体として全体を保持する力め設けているリードフレームを作用する工程、(B)ードフレームの外側端子部側でない面(裏面)に材を設け、円柱状と金型により、外周する内側端子部とを接続する導絡部とは導絡部に力加する位置に設

けられた材料をとりはら、リードフレームのなかり
かれた部分にエッチング液を塗布することにして、
に厚さを付して、リードフレーム全体をエッチング
する工程。(C)リードフレームの表面をむき不
潔の部分を取りはら、電極よりの部分にエッチング液を塗布する工程。

(D) 本装置主子の電子線と、切取されて、本装置子へ照射された内磁電子線の光線とをフレイベンティン
グした後に、所定により外磁電子線区のみを本区に引出
させて全体を封止する工程、(E) 上記外区に引出した
外磁電子線区に本区からなる外磁電場を付与する工程、
を含むことを特徴とする所定封止型本装置の製造
方法。

(見明の江はな氏明)

(0 0 0 1)

(産業上の利用分野) 本発明は、半導体素子を含む回路の封止用の半導体パッケージ（プラスチックパッケージ）に關し、特に、高品質性を向上させ、かつ、多ピン化に対応できる半導体装置とその封止方法に關する。

(0 0 0 2)

10 (LSIの展開) 近年、半導体装置は、高集積化、小型化、低消費電力化と電子回路の高性能化と省資源化の傾向(時代)から、LSIのASICに代替されるように、ますます高集積化、高機能化になってきている。これに伴い、リードフレームを用いた封止型の半導体装置パッケージングにおいて、その成長のトレンドが、SOJ(Small Outline)-Lead PackageやQFP(Quad Flat Pack)のような表面実装型のパッケージを経て、TSOP(Tin Small Outline Package)の普及による薄型化を主軸としたパッケージの小型化へ、さらにはパッケージ内部の3次元化によるチップ収容効率向上を目的としたLOC(Load On Chip)の流通へと進展してきた。しかし、密着封止型半導体装置パッケージには、高集積化、高機能化とともに、更に一層の多ピン化、薄型化、小型化が求められており、上記従来のパッケージにおいてもチップ外部部分のリードの引き出しがあるため、パッケージの小型化に限界が見えてきた。また、TSOP等の小型パッケージにおいては、リードの引き出し、ピンピッチから多ピン化に対しても限界が見えてきた。

(0 0 0 3)

【説明が解決しようとする課題】上記のように、更なる
 廃部封止型半導体装置の高集積化、多機能化が求めら
 れており、新部封止型半導体装置パッケージの層の多
 層化、層型化、小型化が求められている。本発明は、こ
 のような状況のもと、半導体装置パッケージサイズにお
 けるチップの占有率を上げ、半導体装置の小型化に対応
 させ、回路基板への実装密度を低減でき、即ち、回路
 基板への実装密度を向上させることができる新部封止型
 半導体装置を提供しようとするものである。また、回路

に従来の T S O P 系の小型パッケージに搭載であった更なる多ピン化を実現しようとするものである。

(0 0 0 4)

【課題を解決するための手段】本発明の積層型半導体装置は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ突出して外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした積層のリード部とを、絶縁性層を介して、露出して設けており、且つ、絶縁性層への突出のための半田からなる外部電極を前記外部端子部の外部端子部に露出させ、少なくとも前記半田からなる外部電極の一部は接続部より外部に突出させて設けていることを特徴とするものである。尚、上記において、内部端子部と外部端子部とを一体とした積層のリード部の配列を半導体素子の端子側面に二次元的に配列し、外部端子部を半田ボールにて形成することにより B C A (B o i l C o i d A r r a y) タイプの積層型半導体装置とすることとする。

(0 0 0 5) そして、上記において、半導体素子の端子は半導体素子の端子側の面の一列の辺の周中心部上に設けて配列されており、リード部は複数の端子を挟むように対向し前記一列の辺に設けられていることを特徴とするものである。また、本発明のリードフレームは、積層型半導体装置用のリードフレームであって、半導体素子の端子と電気的に接続するための内部端子部と、外部端子部とを連結するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から突出する一方向側に出させ、対向し先導部同士で接続部を介して接続する一方の内部端子部を露出させて設けており、且つ、各外部端子部の外側で、接続リード部と露出し、一体として全体を保持する外部部を設けていることを特徴とするものである。尚、上記リードフレームにおいて、内部端子部と外部端子部とそれらを連結する接続リード部とを一体とした積層のリード部をリードフレーム面に二次元的に配列するとして形成することにより B C A (B o i l C o i d A r r a y) タイプの積層型半導体装置用のリードフレームとすることとする。

(0 0 0 6) 本発明の積層型半導体装置の製造方法は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ突出して外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした積層のリード部とを、絶縁性層を介して、露出して設けており、且つ、絶縁性層への突出のための半田からなる外部電極を前記外部端子部の各リードの外部端子部に露出させる工程を有する。

【作用】本発明の積層型半導体装置は、上記のような構成にすることにより、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応できるものとしている。即ち、半導体装置の内部端子部への突出電極を露出し、絶縁性層への突出電極の向上を可能としている。詳しくは、内部端子部、外部端子部とを一体とした積層のリード部を半導体素子側に地絡させることで安定し、前記外部端子部に半田からなる外部電極を露出させていることにより、装置の小型化を達成している。そして、上記半田からなる外部電極部を、半導体素子面に均等な形で二次元的に配列することにより、半導体装置の多ピン化を可能としている。半田からなる外部電極部を半田ボールとし、二次元的には外部電極部を配列した場合には B C A タイプとなり、半導体装置の多ピン化にも対応できる。また、上記において、半導体素子の端子が半導体素子の端子側の面の一列の辺の周中心部上に設けて配列され、リード部は複数の端子を挟むように対向し前記一列の辺に設けられており、簡単な構造とし、製造性に優れた構造としている。本発明のリードフレームは、上記のような構成にすることにより、上記積層型半導体装置の製造を可能とするものであるが、通常のリードフレームと同様のエッチ

(0 0 0 7)

【作用】本発明の積層型半導体装置は、上記のような構成にすることにより、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応できるものとしている。即ち、半導体装置の内部端子部への突出電極を露出し、絶縁性層への突出電極の向上を可能としている。詳しくは、内部端子部、外部端子部とを一体とした積層のリード部を半導体素子側に地絡させることで安定し、前記外部端子部に半田からなる外部電極部を露出させていることにより、装置の小型化を達成している。そして、上記半田からなる外部電極部を、半導体素子面に均等な形で二次元的に配列することにより、半導体装置の多ピン化を可能としている。半田からなる外部電極部を半田ボールとし、二次元的には外部電極部を配列した場合には B C A タイプとなり、半導体装置の多ピン化にも対応できる。また、上記において、半導体素子の端子が半導体素子の端子側の面の一列の辺の周中心部上に設けて配列され、リード部は複数の端子を挟むように対向し前記一列の辺に設けられており、簡単な構造とし、製造性に優れた構造としている。本発明のリードフレームは、上記のような構成にすることにより、上記積層型半導体装置の製造を可能とするものであるが、通常のリードフレームと同様のエッチ

とが得られ、二層の導電性層を形成する。この形成方法は、上記リードフレームを用いて、リードフレームの内部導電部でない面（裏面）に接地層を形成し、接地層を金メッキにより、方向する内部導電部を形成する導電層とは導電部に対応する位置に設けられた接地層とを形成し、リードフレームの形成された部分が半導体素子の端子部にくるようにして、形成層を介して、リードフレーム全体を半導体素子へ接続し、リードフレームの外周部を含む部分の接地層を接地層を金メッキすることにより、内部導電部と外部導電部を一体化した構造を多層半導体素子上に形成した。本発明の、半導体素子の小型化が可能な、且つ、多ピン化が可能な接続防止型半導体素子の構造を説明している。

(0 0 0 8)

(実施例) 本発明の接続防止型半導体素子の実施例を以下、図にそって説明する。図 1 (a) は本実施例の接続防止型半導体素子の断面図であり、図 1 (b) は素子の平面図である。図 1 中、1 0 0 は接続防止型半導体素子、1 0 1 は半導体素子、1 0 2 はリード部、1 0 2 A は内部導電部、1 0 2 B は外部導電部、1 0 2 C は形成リード部、1 0 1 A は端子部（パッド部）、1 0 3 はワイヤ、1 0 4 は接地層、1 0 5 は形成層、1 0 6 は半田（ペースト）からなる外部電極である。本実施例の接続防止型半導体素子は、前述するリードフレームを用いたもので、内部導電部 1 0 2 A、外部導電部 1 0 2 B を一体化した平型のリード部 1 0 2 を多層半導体素子 1 0 1 上に接地層 1 0 4 を介して形成し、且つ、外部導電部 1 0 2 B 先に半田からなる外部電極を形成部 1 0 5 より外部へ突出させて設けた。パッケージ構造が半導体素子の面側に形成する接続防止型半導体素子であり、図 1 (a) に示すように、半導体素子 1 0 1 の端子部（パッド部）1 0 1 A は半導体素子の中心部より外向して設けられ、中心部 1 0 1 に対して形成されており、リード部 1 0 2 は、内部導電部 1 0 2 A が形成端子部（パッド部）1 0 1 A に接した位置に半導体素子 1 0 1 の面の外側に中心部を向き対向するように形成されている。外部導電部 1 0 2 B は内部導電部 1 0 2 A から形成リード部 1 0 2 C を介して形成されており、半導体素子の形成面に形成した位置で半導体素子部に形成する方向に、形成リード部 1 0 2 C がしきりに金メッキ、外部導電部 1 0 2 B はその先に形成し、半導体素子の面に平面的な方向で一元的に形成している。即ち、中心部 1 0 1 を挟み 2 層の形成層 1 0 2 B の配向を設けている。そして、外部導電部 1 0 2 B に形成させ、半田（ペースト）からなる外部電極 1 0 5 を形成部 1 0 5 より外部へ突出させて設けている。

1. 接地層 1 0 4 としては、1 0 0 μ m 厚のポリイミド系の熱可塑性樹脂 M M 1 2 2 C (日本化成株式会社

と製) を用いたが、他には、シリコンエポキシイミド (T A 1 1 5 (住友ヘーテック株式会社)) や有機化学物質 H C 5 2 0 0 (住友化学株式会社) 等が用いられる。上記実施例では、半田ペーストからなる外部電極であるが、この部分は半田ボールに代えてもよい。尚、本実施例の接続防止型半導体素子は、上記のように、パッケージ構造が半導体素子の面側に形成する、面側に小型化されたパッケージであるが、形成方向については、1 0 m m 以下にすることができ、形成方向 1 0 m m 以下にすることができ、本実施例においては形成層 1 0 5 を、半導体素子の端子部（パッド部）1 0 1 A に形成したが、半導体素子の端子部の位置を二次元的に形成し、内部導電部と外部導電部との一体化となった構造を形成し、半導体素子の端子部に二次元的に形成して形成することにより、半導体素子の、一層の多ピン化に十分対応できる。

(0 0 0 9) 次いで、本発明のリードフレームの実施例を説明し、図 2 にそって説明する。本実施例のリードフレームは、上記実施例の半導体素子に用いられたものである。図 2 は本実施例のリードフレームの断面図を示すもので、図 2 中、2 0 0 はリードフレーム、2 0 1 は内部導電部、2 0 2 は外部導電部、2 0 3 は形成リード部、2 0 4 は接地層、2 0 5 は外部電極である。リードフレームは 4 2 合金 (N i 4 2 % の F e 合金) からなり、リードフレームの厚さは、内部導電部の厚さより厚く 0. 0 5 m m、外部導電部の厚さより厚く 0. 2 m m である。内部導電部の方向する先端部を導電部 2 0 5 まで形成し、0. 0 5 m m 厚に形成されており、前述する半導体素子を形成する際の形成層を形成する層の厚さを金メッキにより形成されている。本実施例では外部導電部 2 0 2 は形成層であるが、これに形成はされない。また、リードフレーム 2 0 0 として 4 2 合金を用いたがこれに形成されない。銅合金でもよい。

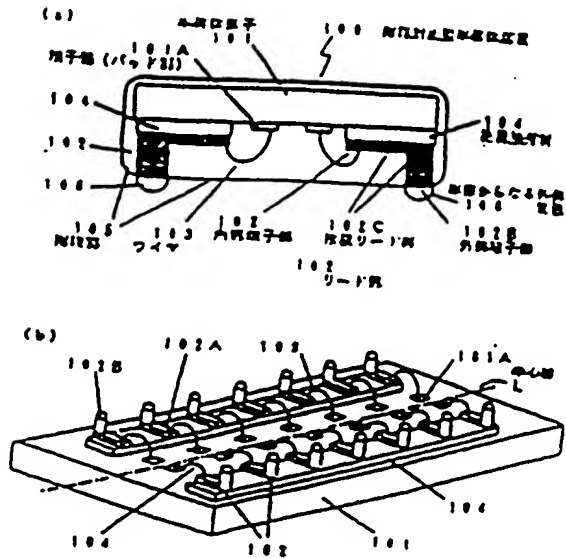
(0 0 1 0) 次に、上記実施例のリードフレームの製造方法を図を用いて簡単に説明する。図 3 は本実施例のリードフレームを製造した工程を示したものである。先ず、4 2 合金 (N i 4 2 % の F e 合金) からなり、厚さ 0. 2 m m のリードフレーム 3 0 0 を形成し、図 3 (a) は、リードフレーム 3 0 0 の両面に形成したレジスト 3 0 1 を形成し、形成した。(図 3 (b))。

次いで、リードフレーム 3 0 0 の両面から所定のパターンを形成してレジストの所定の部分のみを除去を行った後、形成層を形成し、レジストパターン 3 0 1 A を形成した。(図 3 (c))

本レジストとしては、日本化成株式会社製のネガ型レジスト (P M E K レジスト) を使用した。次いで、レジストパターン 3 0 1 A を形成層として、5 7 ° C、4 8 時間の酸化還元処理を経て、リードフレーム 3 0 0 の両面からスプレーエッチングして、形成層

303A 内装端子部
303B 外装端子部
304 送信部
305 金メッキ部
306 外装部
400 リードフレーム
401 絶縁保護材(テープ)
402 外装端子部
403 送信部

(図1)

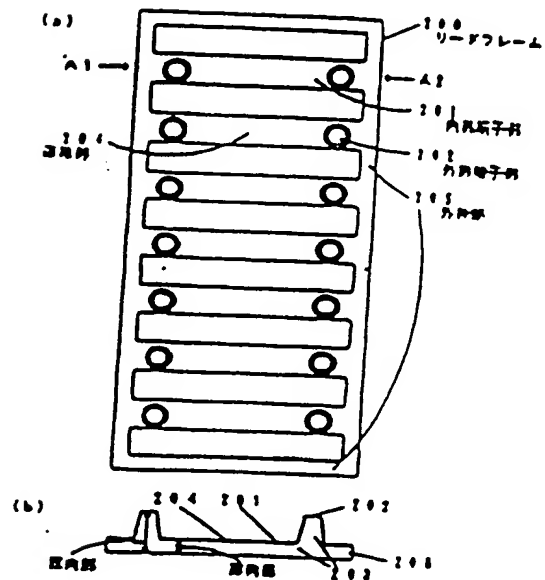


(6)

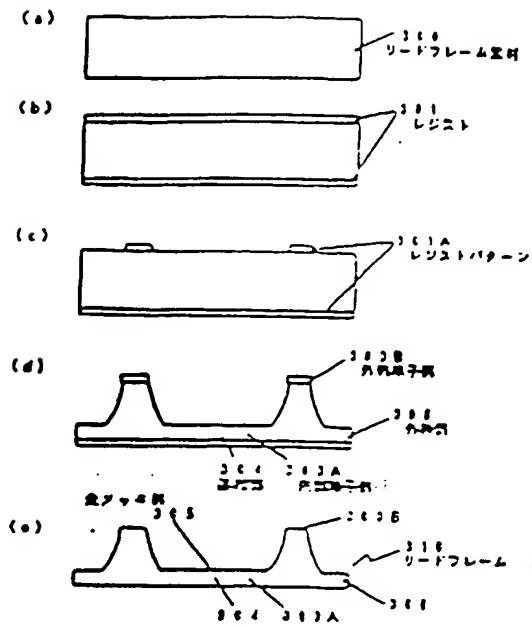
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405A, 405E 1750222
406A, 406B 1750222
410 リード部
410A 内装端子部
410B 外装端子部
410C 絶縁保護材
411 外装端子部
411A ワイヤ
415 送信部

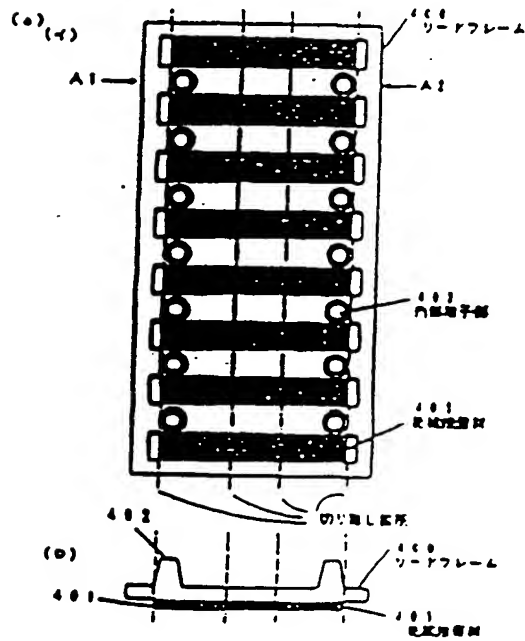
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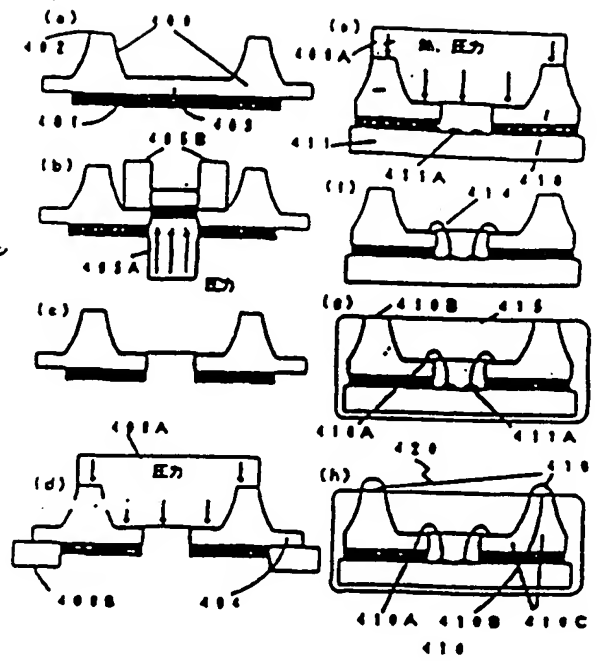
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Japanese Patent Laid-Open Publication No. Heisei 8-125066

[TITLE OF THE INVENTION]

Resin Encapsulated Semiconductor Device, Lead Frame
5 Used Therein, and Fabrication Method for the Resin
Encapsulated Semiconductor Device

[CLAIMS]

1. A resin encapsulated semiconductor device
10 comprising:

a semiconductor chip;

a plurality of leads fixedly attached to a terminal-
end surface of the semiconductor chip by an insulating
adhesive interposed between the semiconductor chip and the
15 leads, each of the leads including integral portions, that
is, an inner terminal portion adapted to be electrically
connected to an associated one of terminals of the
semiconductor chip, an outer terminal portion extending
outwardly in a direction orthogonal to the terminal-end
20 surface of the semiconductor chip and adapted to be
connected to an external circuit, and a connecting lead
portion adapted to connect the inner and outer terminal
portions to each other; and

outer electrodes each connected to the outer terminal
25 portion of an associated one of the leads and made of

solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate.

5 2. The resin encapsulated semiconductor device according to claim 1, wherein the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip,
10 and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets.

15 3. A lead frame comprising:
 a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to
20 be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other;

 each of the outer terminal portions of the leads
25 being protruded in a direction orthogonal to a lead frame

surface via an associated one of the connecting lead portions;

the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively;

connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and

an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame.

4. A method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive-interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit,

and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow
5 the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of:

(A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner
10 terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and
15 outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a
20 fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the
25 connecting lead portions in such a fashion that they form

an integral structure together, thereby protecting the entire portion of the lead frame;

(B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween;

(C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions;

(D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and encapsulating the semiconductor chip and the lead frame by a resin while allowing a surface of the lead frame toward the outer terminal portions to be externally exposed; and

(E) forming outer electrodes made of solder on the exposed lead frame surface toward the outer terminal portions.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin encapsulated semiconductor device (plastic package) in which a semiconductor chip is packaged, and more particularly to a semiconductor device configured to achieve an improvement in mounting density or to have a multi-pinned structure and a method for manufacturing such a semiconductor device.

10 [DESCRIPTION OF THE PRIOR ART]

Recently, semiconductor devices have been developed to have a higher integration degree and a higher performance by virtue of developments of techniques associated with an increase in integration degree and miniaturization and in pace with the tendency of electronic appliances to have a high performance and a light, thin, simple, and miniature structure. A representative example of such semiconductor devices is an ASIC of LSI. For instance, developments of resin encapsulated semiconductor device plastic packages have been advanced from surface-mounting packages such as SOJs (Small Outlined-Leaded Packages) or QFPs (Quad Flat Packages) to packages having a miniature structure mainly achieved in accordance with a thinness obtained by virtue of developments of TSOPs (Tin Small Outline Packages) or to LOC (Lead On Chip) structures

adapted to achieve an improvement in the chip packaging efficiency by virtue of developments of an internal three-dimensional package structure. In addition to an increase in integration degree and improvement in performance, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In the above mentioned conventional packages, however, there is a limitation in miniaturization because those packages have a structure in which leads are arranged around a chip. Similarly, leads are arranged around a chip in the case of miniature packages such as TSOPs. In such packages, there is also a limitation in increasing the number of pins due to the pin pitch used.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

As mentioned above, there has been demand for an increase in integration degree and improvement in performance of resin encapsulated semiconductor devices. Also, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In such situations, the present invention makes it possible to increase the occupancy degree of a chip in a semiconductor package with a limited size while reducing the mounting area of the

semiconductor package on a circuit board to achieve a miniaturization of the resulting semiconductor device. That is, the present invention is adapted to provide a resin encapsulated semiconductor device capable of achieving an improvement in the mounting density thereof on a circuit board. Also, the present invention is adapted to achieve an increase in the number of pins which is difficult in miniature packages such as conventional TSOPs.

10 [MEANS FOR SOLVING THE SUBJECT MATTERS]

The resin encapsulated semiconductor device of the present invention is characterized in that it comprises: a semiconductor chip; a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the

leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate. The above semiconductor device can be embodied into a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The above semiconductor device is also characterized in that the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. The lead frame of the present invention is characterized in that it comprises: a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be

connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions; the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively; connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame. The above lead frame can be embodied into a lead frame for a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The present invention is also characterized by a method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached

to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of: (A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a

lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame; (B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween; (C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions; (D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and

encapsulating the semiconductor chip and the lead frame by
a resin while allowing a surface of the lead frame toward
the outer terminal portions to be externally exposed; and
(E) forming outer electrodes made of solder on the exposed
5 lead frame surface toward the outer terminal portions.

[FUNCTIONS]

With the above mentioned configuration, the resin
encapsulated semiconductor device of the present invention
10 can increase the occupancy degree of the chip while
achieving a miniaturization thereof. That is, the resin
encapsulated semiconductor device is capable of reducing
the mounting area thereof on a circuit board and achieving
an improvement in the mounting density thereof on the
15 circuit board. In particular, the present invention
achieves a miniaturization of the semiconductor device by
fixedly attaching a plurality of leads each including an
inner terminal portion and an outer terminal portion
integral with each other to a surface of a semiconductor
20 chip by an insulating adhesive layer interposed between the
semiconductor chip and the leads, and connecting outer
electrodes made of solder to the outer terminal portions,
respectively. Also, the present invention achieves an
increase in the number of pins in the semiconductor device
25 by arranging the outer electrodes made of solder in a two-

dimensional fashion on a plane parallel to the surface of the semiconductor chip. Where the outer electrodes made of solder are formed in the form of solder balls and arranged in a two-dimensional fashion, a BGA type semiconductor device capable of achieving an increase in the number of pins can be obtained. In the above semiconductor device, the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. Thus, the semiconductor device has a simple structure suitable in regard to productivity. The lead frame of the present invention makes it possible to fabricate the above mentioned resin encapsulated semiconductor device by virtue of there above mentioned configuration thereof. However, this lead frame can be fabricated using a half etching method during an etching process as used for conventional lead frames. The method for fabricating a resin encapsulated semiconductor device in accordance with the present invention involves the steps of applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out

the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween, and cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions. Thus, a plurality of leads each including an inner terminal portion and an outer terminal portion integral with each other are mounted on a semiconductor chip. Accordingly, the present invention makes it possible to achieve a miniaturization of semiconductor devices. In accordance with the present invention, it is also possible to fabricate a resin encapsulated semiconductor device having an increased number of pins.

(EMBODIMENTS)

Hereinafter, embodiments of the present invention associated with resin encapsulated semiconductor devices will be described in conjunction with the annexed drawings. Fig. 1A is a cross-sectional view schematically

illustrating a resin encapsulated semiconductor device according to an embodiment of the present invention. Fig. 1B is a perspective view illustrating an essential part of the resin encapsulated semiconductor device. Figs. 1A and 5 1B, the reference numeral 100 denotes the resin encapsulated semiconductor device, 101 a semiconductor chip, 102 leads, 102A inner terminal portions, 102B outer terminal portions, 102C connecting lead portions, 101A contacts (pads), 103 wires, 104 an insulating adhesive, 105 a resin encapsulate, 106 outer electrodes made of solder (paste), respectively. The resin encapsulated semiconductor device according to this embodiment is fabricated using a lead frame which will be described hereinafter. In this resin encapsulated semiconductor 15 device, a plurality of L-shaped leads 102, each of which has an inner terminal portion 102A and an outer terminal portion 102 integral with each other, are mounted on a semiconductor chip 101 by means of an insulating adhesive 104. An outer electrode 106, which is made of solder, is 20 attached to each outer terminal portion 102B. The outer electrode 106 is outwardly protruded from a resin encapsulate 105. The resin encapsulated semiconductor device configured as mentioned above has a package area substantially equal to the entire area thereof. When this 25 semiconductor device is mounted on a circuit board, the

solder is melted and then solidified to allow the outer terminal portions 102B to be electrically connected to an external circuit. In the resin encapsulated semiconductor device according to the illustrated embodiment, contacts
5 (pads) 101A provided at the semiconductor chip 101 are arranged in pairs along a center line L of the semiconductor chip 101 at opposite sides of the center line L in such a fashion that contacts included in each contact pair face each other. The outer terminal portion 102B of
10 each lead is spaced apart from the inner terminal portion 102A of the lead. Between the inner and outer terminal portions 102A and 102B, a connecting lead portion 102C is interposed. The connecting lead portion 102C of each lead is bent in a direction orthogonal to the major surface of
15 the semiconductor chip at a position near an associated one of the side surfaces of the semiconductor chip 101, so that it has an L shape. In each lead, the outer terminal portion 102B is arranged at an end of the connecting lead portion 102C. The outer terminal portions 102B of the
20 leads are arranged in a one-dimensional fashion on a plane parallel to the major surface of the semiconductor chip 101. That is, the outer terminal portions 102B are arranged in two lines at opposite sides of the center line L. As mentioned above, one outer electrode 106 made of
25 solder is connected to the outer terminal portion 102B of

each lead and outwardly exposed from the resin encapsulate
105.

For the insulating adhesive 104, a polyimide-based thermoplastic adhesive having a thickness of 100 μm (HM122C
5 manufactured by Hitachi Chemical Co., Ltd.) is preferably used. Alternatively, a silicon denaturalized polyimide adhesive (ITA1715 manufactured by Sumitomo Bakelite Co., Ltd.) or a thermosetting adhesive (HG5200 manufactured by Tomoeokawa Papermaking Co., Ltd.) may be used. Although
10 outer electrodes made of solder paste are used in the illustrated embodiment, solder balls may be used.

As mentioned above, the resin encapsulated semiconductor device according to the illustrated embodiment has a package area substantially equal to the
15 entire area thereof. That is, the illustrated embodiment of the present invention provides a package having a compact structure in regard to area. In accordance with the present invention, a thinned package structure can also be provided in that it is also possible to reduce the
20 package thickness to about 1.0 mm or less. Although the outer electrodes have been described as being arranged in two lines along the contacts (pads) of the semiconductor chip, they may be arranged in a two-dimensional fashion. This is achieved by arranging contacts of the semiconductor
25 chip in a two-dimensional fashion. On the surface of the

semiconductor chip arranged with those contacts, a plurality of terminal sets each having an inner terminal and outer terminal integral with each other are arranged in a two-dimensional fashion. In this case, it is possible to
5 fabricate a semiconductor device using a semiconductor chip with an increased number of pins.

An embodiment of the present invention associated with a lead frame will now be described. The lead frame according to this embodiment is adapted to be used in the
10 above mentioned semiconductor device. Fig. 2 is a plan view of the lead frame according to this embodiment. In Fig. 2, the reference numeral 200 denotes a lead frame, 201 inner terminal portions, 202 outer terminal portions, 203 connecting lead portions, 204 a connecting portion, and 205
15 an outer frame portion, respectively. The lead frame is made of 42 ALLOY (namely, an Fe alloy containing 42% Ni). The lead frame has a thickness of 0.05 mm at its thinner portion, that is, the inner terminal portions, and a thickness of 0.2 mm at its thicker portion, that is, the
20 outer terminal portions. The connecting portion, which connects facing tips of the inner terminal portions to each other, has a thickness of 0.05 mm corresponding to that of the thinner portion. This connecting portion has a
25 structure capable of allowing an easy punching thereof in the fabrication of the semiconductor device, as described

hereinafter. Although the outer terminal portions 202 have a ball shape in the illustrated embodiment, they are not limited to this shape. Also, although the lead frame has been described as being made of the 42 ALLOY, it is not limited to this material. For the lead frame, a copper-based alloy may be used.

Now, fabrication of the lead frame according to the illustrated embodiment will be described in brief. Fig. 4 illustrates a process for fabricating the lead frame according to the illustrated embodiment. First, a lead frame blank 300 having a thickness of 0.2 mm was prepared which is made of a 42 ALLOY (an Fe alloy containing 42% Ni). The prepared lead frame blank 300 was then subjected to a cleaning process, thereby removing grease from the surfaces thereof (Fig. 3a). Subsequently, photoresist films 301 were coated over both surfaces of the lead frame blank 300, respectively. The coated photoresist films 301 were then dried (Fig. 3b).

Using desired pattern plates, the photoresist films 301 on both surfaces of the lead frame blank 300 were exposed to light at their desired portions. A developing process was then conducted to the light-exposed photoresist films 301, thereby forming photoresist patterns 301A.

For the photoresist films, a negative liquid-phase resist (PMER resist) manufactured by Tokyo Ohka Co., Ltd.

was used. Using the resist patterns 301A as anti-etch films, the lead frame blank 300 was subjected to a spray etching process at both surfaces thereof. The spray etching process was conducted using a ferric chloride solution of 48 BAUME at 57 °C. Thus, a lead frame having a structure of Fig. 2a was obtained (Fig. 3d). Fig. 2a is a plan view of the lead frame. Fig. 2b is a cross-sectional view taken along the line A1 - A2 of Fig. 2a. Thereafter, the remaining photoresist thin films were peeled off. The resulting structure was then subjected to a cleaning process. A gold plating process was subsequently conducted for desired portions of the lead frame, that is, regions including inner terminal portions (Fig. 3e).

In the fabrication process of the lead frame, the etching process was conducted with a large etch depth at one major surface of the lead frame blank where outer terminal portions are to be formed, and with a small etch depth at the other major surface of the lead frame. In place of the gold plating, silver or palladium plating may be utilized. The above mentioned lead frame fabrication process is adapted to manufacture a single lead frame required for the manufacture of a single semiconductor device. In terms of productivity, however, the etching process is conducted for lead frame units each corresponding to the single lead frame shown in Fig. 2. To

this end, a frame member (not shown) is provided at a desired portion of the peripheral edge of the lead frame so as to connect a desired part of the outer frame portion 205 shown in Fig. 2 to a corresponding one of an adjacent lead frame.

Using the lead frame fabricated as mentioned above, the resin encapsulated semiconductor device according to the present invention was fabricated. Now, a method for fabricating the resin encapsulated semiconductor device in accordance with an embodiment of the present invention will be described. Fig. 4 illustrates the method for fabricating the resin encapsulated semiconductor device in accordance with the embodiment of the present invention. A polyimide-based thermosetting insulating adhesive (tape) 401 (HM122C manufactured by Hitachi Chemical Co., Ltd.) was applied to one surface, formed with the outer terminal portions 402, of the lead frame 400 fabricated as in Fig. 3 and the outer surface of the lead frame 400 using a hot pressing process conducted at 400 °C and 6 Kg/m² for 1.0 second (Fig. 4a). The resulting structure is shown in Fig. 5 which is a plan view. Thereafter, the connecting portions 403 connecting facing tips of the inner terminal portions were punched using punching dies 405A and 405B (Fig. 4b). Also, portions of the insulating adhesive

(tape) corresponding to those connecting portions 403 were punched (Fig. 4c).

Subsequently, unnecessary portions of the lead frame including the outer frame 404 were cut off using outer frame punching and pressing dies 406A and 406B (Fig. 4d).
5 The lead frame was then bonded to a semiconductor chip 407 at its leads 410 under pressure while applying heat (Fig. 4e).

The process for cutting off the unnecessary portion
10 of the lead frame including the outer frame 404 supporting the entire portion of the lead frame along with the connecting lead portion, as shown in Fig. 4d, may be carried out after an resin encapsulating process. In this case, dam bars (not shown) are preferably provided, as in
15 QFP packages typically using a lead frame having a single layer structure. After the mounting of the leads 410 on the semiconductor chip 411, the inner terminal portion 410 of each lead 410 was electrically connected to an associated one of terminals (pads) 411A of the
20 semiconductor chip 411 (Fig. 4f).

Subsequently, an epoxy-based resin 415 was molded to encapsulate the resulting structure while exposing the outer terminal portions 410B of the leads 410 using a desired mold (Fig. 4g).

Although a specific mold (not shown) was used for the above process in the illustrated case, use of such a die may be unnecessary in so far as the resin encapsulating process can be conducted under the condition in which
5 desired portions (outer terminal portions) of the lead frame are left. Thereafter, a solder paste was coated on the exposed outer terminal portions 410B in accordance with a screen printing process, thereby forming outer electrodes
10 416 made of solder (paste). Thus, the fabrication of the resin encapsulated semiconductor device according to the present invention was achieved (Fig. 4h).

Although the formation of the outer electrodes 416 made of solder has been described as being achieved using a screen printing process, it may be achieved using a reflow
15 or bonding process in so far as an amount of solder required for a connection of the semiconductor device to a circuit board is obtained.

[EFFECTS OF THE INVENTION]

20 As apparent from the above description, the present invention makes it possible to increase the occupancy degree of a semiconductor chip in a semiconductor package in situations requiring new resin encapsulated
25 semiconductor devices having a highly integrated structure while exhibiting a high performance. The present invention

also makes it possible to reduce the area of the semiconductor device on a circuit board in order to cope with a compactness of the semiconductor device. That is, the present invention can provide a semiconductor device
5 capable of achieving an improvement in the mounting density on a circuit board. At the same time, the present invention can provide a resin encapsulated semiconductor device having a new multipinned structure which could not be realized in compact packages such as conventional TSOPs.